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| TRANSMITTAL LETTER (General - Patent Pending) | Docket No. 01240190AA |
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In Re Application Of: **A. Watson, et al.**



| Application No. | Filing Date | Examiner | Customer No. | Group Art Unit | Confirmation No. |
|---|---|---|---|---|---|
| 10/711,143 | August 27, 2004 | Unassigned | 46170 | 2825 | 5142 |

Title: **METHODOLOGY OF QUANTIFICATION OF TRANSMISSIN PROBABILITY FOR MINORITY CARRIER COLLECTION IN A SEMICONDUCTOR CHIP**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**INFORMATION DISCLOSURE STATEMENT; PTO-1449; 9 DOCS**

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.
  - ☐ Charge the amount of
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.
- ☐ Payment by credit card. Form PTO-2038 is attached.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

*Signature*

Dated: **October 8, 2004**

**Michael E. Whitham**
**Reg No. 32,635**
**Whitham, Curtis & Christofferson, P.C.**
**11491 Sunset Hills Road, Suite 340**
**Reston, Virginia 20190**
**703-787-9400**

CC:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

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*Signature of Person Mailing Correspondence*

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*Typed or Printed Name of Person Mailing Correspondence*

(01240190AA)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

A. Watson, et al.

Serial No.: 10/711,143 Group Art Unit: 2825

Filed: August 27, 2004 Examiner: Unassigned

For: METHODOLOGY OF QUANTIFICATION OF TRANSMISSION PROBABILITY FOR MINORITY CARRIER COLLECTION IN A SEMICONDUCTOR CHIP

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Under the provisions of 37 C.F.R. §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. §1.56, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner.

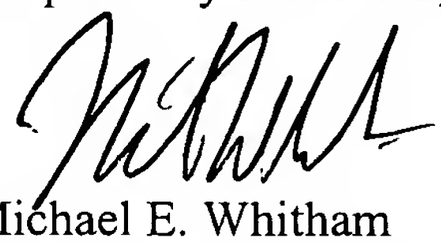
This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

(01240190AA)

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,



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11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190
703-787-9400
Customer number: 45773

# INFORMATION DISCLOSURE CITATION

*(Use several sheets if necessary)*

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|---|---|
| BUR920040120US1 | 10/711,143 |
| **Applicant(s)** A. Watson, et al. | |
| **Filing Date** August 27, 2004 | **Group Art Unit** 2825 |

## U.S. PATENT DOCUMENTS

| *EXAMINER INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
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## FOREIGN PATENT DOCUMENTS

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| | | JP2020039 | | Japan | | abstract | ✓ | |
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**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

| | | |
|---|---|---|
| | | SUBSTRATE MODELING AND LUMPED SUBSTRATE RESISTANCE EXTRACTION FOR CMOS ESD/LATCHUP CIRCUIT SIMULATION, T. Li, et al., Coordinated Science Laboratory, Dept. of Electrical and Computer Engineering University of Illionois at Urbana-Champaign, Urbana, IL (1999) |
| | | BIPOLAR TRANSISTOR ACTION AND TRANSPORT EFFECTS RELATING TO CMOS LATCHUP, G. Krieger, IEEE Transactions on Electron Devices, Vol. ED-34, No. 8, August 1987, pgs. 1719-1728 |

| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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## OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

| | | |
|---|---|---|
| | | PARASITIC LATERAL BIPOLAR TRANSISTORS IN CMOS, L. Deferm, et al., Solid-State Electronics, Vol. 32 No. 2, pgs 103-109, 1989 |
| | | A NEW ANALYTICAL THREE-DIMENSIONAL MODEL FOR SUBSTRATE RESISTANCE IN CMOS LATCHUP STRUCTURES, M. Chen, et al., IEEE Transactions on Electron Devices, Vol. ED-33 No. 4 pgs. 489-493, April 1986 |

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## OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

| | | |
|---|---|---|
| | | STATIC AND TRANSIENT LATCHUP SIMULATION OF VLSI-CMOS WITH AN IMPROVED PHYSICAL DESIGN MODEL, M. Strzempa-Depre, et al., IEEE Transactions on Electron Devices, Vol. ED-34 No. 6, June 1987, pgs 1290-1296 |
| | | A CMOS MODEL FOR COMPUTER-AIDED CIRCUIT ANALYSIS AND DESIGN, J. W. Roberts, et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989, pgs 128-138 |

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**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*

| | | |
|---|---|---|
| | | CORRELATING THE CHANNEL, SUBSTRATE, GATE AND MINORITY-CARRIER CURRENTS IN MOSFETs, C. Hu et al., IEEE International, Solid-State Circuits Conference, Digest of Technical Papers February 1983, pgs. 88-90 |
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